

IXO-HXI Technology Development Roadmap

ver. 2009.07.19 The IXO-HXI team

Title : HXI Technology development roadmap

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1 INTRODUCTION

1.1 Requirements and Instrument concept

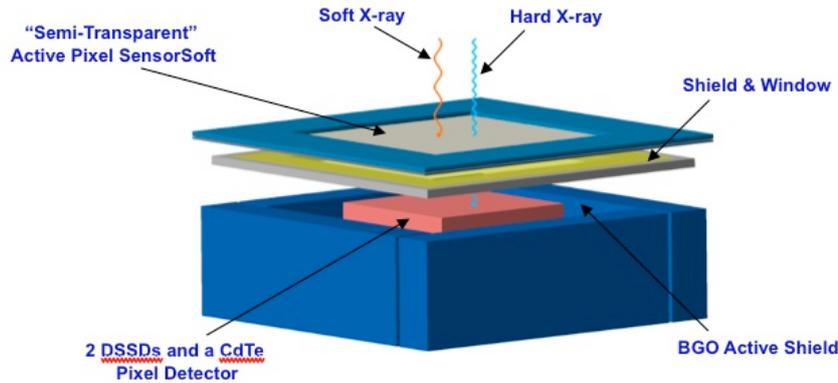


Figure 1. WFI/HXI concepts.

Table 1: Requirements on the HXI

Energy Range	10—40 keV
Angular Resolution (")	<30 (goal 5 for over sampling) @ 10-40 keV
Field of View (°)	8 x 8 @ 10-40 keV
Spectral Resolution (eV: FWHM)	1000 @ 10-40 keV
Detection efficiency	> 90% up to 40 keV
Position Resolution (mm)	< 3 (goal 0.25 for oversampling)
Detector area	> 47 mm square

The Hard X-ray Imager (HXI) is to be mounted beneath the Wide Field Imager (WFI), to extend the energy range of IXO up to 40 keV. The HXI is required to cover from 10 keV to 40 keV with an energy resolution better than 1 keV (FWHM). The area required to be covered by the HXI is 8×8 arcmin².

In order to achieve wide-band up to 40 keV with high sensitivity, high resolution imaging spectroscopy, HXI consists of an imaging spectrometer based on advanced technologies of the Cadmium Telluride (CdTe), and two (or more) layers of Si-based imaging spectrometer covering up to ~25 keV. BGO (Bi₄Ge₃O₁₂) scintillating crystals surrounding the imager is also essential to achieve lower background and hence higher sensitivity. A baffle system to diminish the Cosmic X-ray Background (CXB) incoming from other direction than the mirror becomes important, as well.

There are a few hard X-ray imaging missions which will be launched in orbit in advance to IXO, such as NuSTAR (NASA led) and ASTRO-H (JAXA led). The HXI on IXO will incorporate lessons learned from these development activities. The IXO-HXI system at present is base mainly on the ASTRO-H HXI system as a reference, and incorporating experiences from the

other missions. ASTRO-H is currently in phase-B, and planned to be launched at 2013 (in Japanese Financial Year), well advanced to the IXO project.

1.2 Instrument design

The HXI system as a whole is attached to the WFI system. The HXI part composes of 3 boxes, the sensor assembly (HXI-S), the analog electronics box (HXI-E) and the digital electronics box (HXI-D).

HXI-S mainly composes of

- Two Double-sided Si Strip Detectors (DSSDs) with 47x47 mm size, 0.5 mm (TBR) thickness and associated front-end electronics including analog ASICs (application specific integrated circuits) in particular. High voltage bias generator (HVs) are also associated. The imagers will be controlled via specific FPGAs (field programmable gate arrays), installed with control logics.
- A Double-sided Strip CdTe Detector (DS-CdTe) or a CdTe pixel imager with 47x47 mm size in total, and 0.5 mm (TBR) thickness, and associated front-end electronics including analog ASICs in particular. High voltage bias generator (HVs) are also associated. The imagers will be controlled via specific FPGAs (field programmable gate arrays), as well, installed with control logics.
- BGO active shield crystals read-out via Avalanche Photo Diodes (APDs), with associated charge sensitive amplifier (CSA) and electronics including analog-to-digital converters (ADCs). High voltage bias generator (HVs) are also associated. The detectors will be controlled via specific FPGAs (field programmable gate arrays), installed with control logics.
- A house keeping (HK) logic board accumulating, e.g. temperature with ADCs and drivers for heater control.

HXI-E mainly composes of

- Data handling logic boards with FPGAs, interfacing with the DSSDs, DS-CdTe (or CdTe pixel), BGOs and the HK board to accumulate observational data. It is also connected to HXI-D
- A power supply unit (PSU) board with DC-DC converters and control logics, for its own and HXI-S power.

HXI-D mainly composes of

- CPU board connected to the logic boards on HXI-E. Compiles the telemetry data and communicates with space-craft network.
- A power supply unit (PSU) board with DC-DC converters and control logics for its own power.

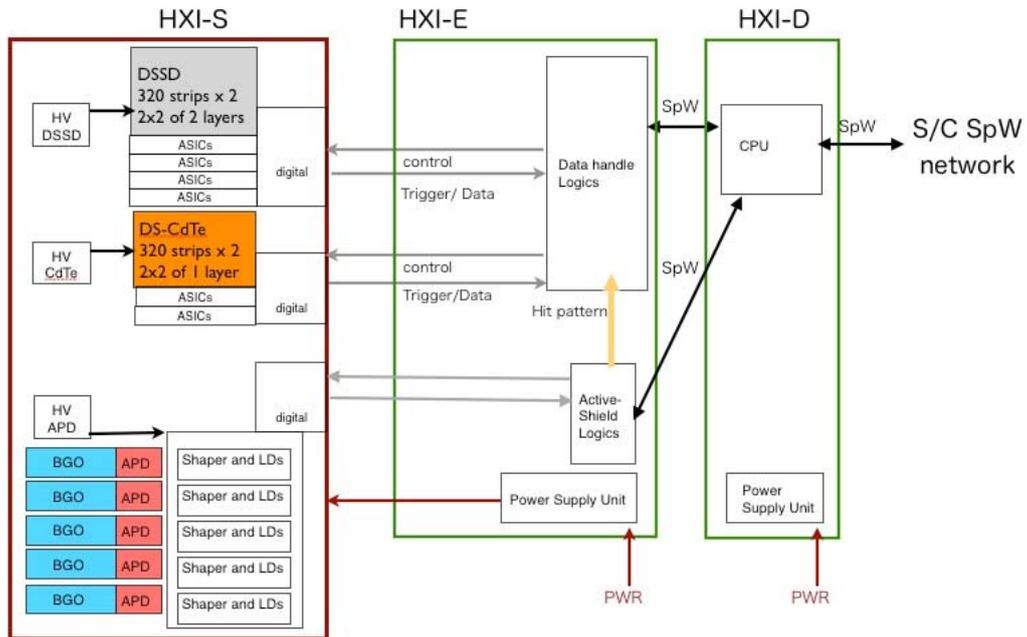


Figure 2. Overview of the sub-system of HXI

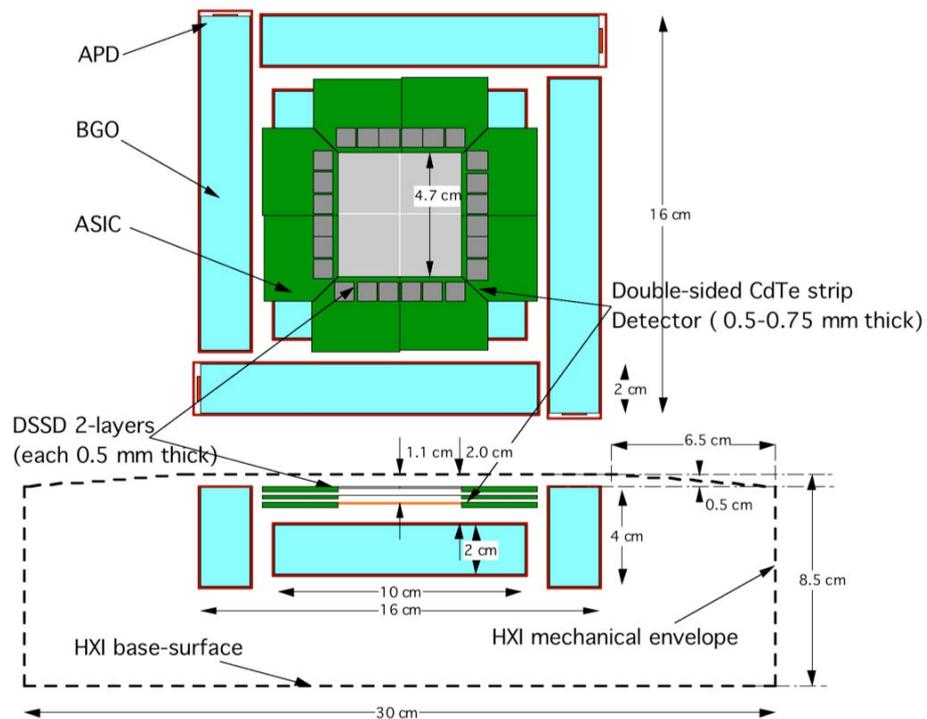


Figure 2. HXI-S concept design.

2 TECHNICAL STATUS

Current technical status of the imager part with its associated electronics is summarized in table 2. On the CdTe imager, only the strip option (base-line) case is shown for simplicity.

Table 2: Specification and status of imager technologies

Requirement	Specification	Comments	Achieved
CdTe imager Area	47 x 47 mm ²	Could be a single 47 mm detector, or in 2x2 tiled configuration	12.5 mm and 25 mm wide devices in operation
CdTe Thickness	0.5 mm	Could be 0.75 mm depending on trade-offs.	12.5 mm wide device with 0.5 and 0.75 mm thickness in operation
Pixel size	0.25 mm	ASTRO-H HXI default is 0.25 mm.	12.5 mm wide device with 0.25 mm resolution in operation
Array dimensions	192 + 192 strips	orthogonally implemented in front and in back	64 + 64 prototype in operation.
Energy resolution	< 1 keV at 30 keV	In FWHM	1.2 keV at 32 keV achieved
DSSD Thickness	0.5 mm		25, 32 and 39 mm wide device with 0.5 mm thickness in operation
Pixel size	0.25 mm	ASTRO-H HXI default is 0.25 mm.	32 mm wide device with 0.25 mm resolution in operation
Array dimensions	192 + 192 strips	orthogonally implemented in front and in back	64 + 64 prototype in operation.
Energy resolution	< 1 keV at 30 keV	In FWHM	1.2 keV at 32 keV achieved

Another major concern is the interface between the WFI and the HXI.

–Initial study of thermal cross-talk is to be held this year.

–Electrical cross-talk is designed to be very small; i.e. all the electrical interface is independent. Detailed follow-up investigations will be held on the development phase.

–Background cross-talk, i.e. secondary photons from one part detected in the other part, is designed to be small, using the DSSD layers as a buffer. Will also be checked in detail in the development phase.

Technology of active shielding are summarized as follows:

–Similar BGO crystal has been flown in Suzaku satellite (total 150 kg)

–Similar APD is working in orbit in Cute-1.7 micro satellite

–Similar analog chain is working in orbit in Suzaku satellite (HXD-PIN detectors)

–Breadboard models with 20x15x4 cm³ BGO and 1 cm wide APD successfully operated in laboratory equipment, from the year 2006

–The geometry optimized for IXO orbit is still under study, including the WFI effects.

3 TECHNOLOGY ROADMAP

3.1 Test and verification strategy

The IXO HXI is mainly based on the Hard X-ray Imager on board the ASTRO-H mission (ASTRO-H/HXI). HXI-S of the ASTRO-H is considered as a BBM for IXO (most part is the same in the component level), while HXI-E and -D are as EM for IXO (only minor update is planned). Since ASTRO-H will be launched by 2014 or so, all the function checks will be ended by late-2011, before ASTRO-H goes into phase-C, and performance check as well as qualification check (environment tests and long-term running) will be mostly ended by mid-2011 (TRR-2 of IXO) and perfectly done by early 2012 (delivery to ASTRO-H space craft).

Table 3. Development schedule. ASTRO-H HXI is considered as BBM/EM for IXO counterparts. Development activities lead by the ASTRO-H project, and then fed-back into IXO is hatched with yellow, while IXO-only studies are in green

Name	leading project	2009			2010				2011				2012
		Apr-Jun	Jul-Sept	Oct-Dec	Jan-Mar	Apr-Jun	Jul-Sept	Oct-Dec	Jan-Mar	Apr-Jun	Jul-Sept	Oct-Dec	Jan-Mar
ASTRO-H mile stones		← EM fab / test →			← EM/env. test →				← FM fab / test →				
				^PDR1	^PDR2	← FM design →			^CDR	← FM calibration →			
								▽TRL5					▽TRL6
HXI-S													
DSSD imager	A-H	← A-H/FM DSSD quality →			← A-H EM cal. / env. tests →				← A-H/FM fab →				
		← A-H/EM system fab. →			← A-H/FM func. test / env. tests →								
CdTe imager	A-H	← A-H/FM DS-CdTe quality →			← A-H EM cal. / env. tests →				← A-H/FM fab →				
		← A-H/EM system fab. →			← A-H/FM func. test / env. tests →								
ASIC	A-H	← EM ASIC 1st-lot fab →			← FM ASIC 1st-lot fab. →				← FM ASIC fab. →				
		← EM ASIC spec test →			← FM ASIC spec test →								
active shield detector	A-H	← EM modules fab./env. test →			← EM cal. →				← FM fab. / cal →				
		← EM fab. →			← FM-fab. trial →								
active shield electronics	A-H	← EM fab. →							← FM fab. / cal →				
active shield optimization	IXO	← design tuning →							← On-going tuning →				
HV, DCDC and HV	A-H	← EM fab./env. test →							← FM fab. / cal →				
WFI interface assessment (IXO)	IXO	← design tuning →							← On-going tuning →				
HXI-E													
Digital I/O board		← EM function test →							← FM fab. / cal →				
Power Supply		← EM fab. / env. test →							← FM fab. / cal →				
HXI-D													
CPU board		← EM function test →							← FM fab. / cal →				
Software		← System designing →							← FM fab. / cal →				
		← Reference design coding →											
Power Supply		← EM fab. / env. test →							← FM fab. / cal →				

At the same time, reconfiguration of IXO HXI-S design will be performed till early-2011 to handle larger-size imager, change of orbit and cosmic-ray environment (with smaller BGO anti-coincidence subsystem), and a little lower operation temperature (from -20C at ASTRO-H to -40 or -30 at IXO/HXI). For better energy resolution and risk mitigation, two CdTe imager technologies (double-sided strip and pixel) will be developed and compared, for selection of base-line design around 2011.

3.2 HXI-S

Major technologies:

1. Double-sided Si Strip Detectors (DSSDs) with read-out electronics made around an analog ASICs and logic boards for control.
2. Double-sided Strip CdTe Detector (DS-CdTe) or a CdTe pixel imager (CdTe imager) with read-out electronics made around an analog ASICs and logic boards for control.
3. ASICs
4. BGO active shield crystals read-out via Avalanche Photo Diodes (APDs), with associated charge sensitive amplifier (CSA) and electronics including analog-to-digital converters (ADCs), high voltage bias generator (HVs) and logic boards for control.
5. House keeping (HK) logic board
6. Housing (or casing) structure

Current Status:

For the ASTRO-H project, all the major technologies are in the status of TRL-4. All systems have been successfully operated in laboratory environment.

Future plan (by mid-2011):

For item.3 (ASIC), by mid-2009, we will have a working ASIC and its board, controlled via a logic board, connected to a test Si strip Detector. If no major defect is identified, these ASIC will be considered for flight model of the ASTRO-H/HXI, and back-up solution for the IXO/HXI as well.

For item.1 (DSSD) and 2 (DS-CdTe), following this test, we will build EM (models for electrical test and performance verification) level components for ASTRO-H/HXI, which is the DS-CdTe imager EM and the DSSD imager EM. Energy resolution and imaging qualities will be verified. The qualification (mechanical, thermal and vacuum, if required) tests will be ended by early 2010. Independent work for CdTe pixel imager (item.2) will also be held, to achieve TRL5 by mid-2011, and TRL6 by early 2012.

For item.4 (BGO anti-coincidence subsystem), the mechanical holding structure test model qualification is undergoing. The read-out system using a real-size (for ASTRO-H/HXI) BGO crystal and FM candidate APD also worked well, and mechanical and electrical work will be combined by mid-2009. The BGO-based anti-coincidence sub-system will reach TRL-5 by mid-2011, and TRL6 by early 2012. For IXO, the design tuning of the BGO geometry (including its shape and thickness) will be studied as well, to minimize the background signal detected in DSSDs and CdTe imagers, due mid-2011, with first result presented by mid-2010.

Items.5 (HK) and 6 (housing/casing) is not critical items. Thermal design in combination with WFI-parts will need careful consideration, but a simple coupling estimate shows the heat transfer is less than a few watts.

3.3 HXI-E

The HXI-E is in principle reusing the same design as those of ASTRO-H/HXI, with a few modifications. Thus, it reaches TRL5 by mid-2011, and TRL-6 by early 2012, when the system is delivered to the ASTRO-H spacecraft.

Major technologies:

1. Digital I/O boards (DIO boards) with FPGAs, controlling the front-end electronics of DSSDs and CdTe imager and BGO anti-coincidence subsystem. Control trigger enable, accumulate dead-time information, generate raw data, and send to the CPU board in HXI-D.
2. Power supply unit (PSU) for HXI-E and HXI-S.

Current Status:

For the ASTRO-H project, all the major technologies are in the status of TRL-4. All systems have been successfully operated in laboratory environment.

Future plan (by mid-2011):

EM (models for electrical test and performance verification) units of DIO boards and PSU are be fabricated and will be tested by early-2010. Function test as well as qualification tests (thermal, and if required, vacuum and mechanical) will be performed by mid-2010.

ASTRO-H/FM fabrication will start at late-2010, and basic function test will be done by mid-2011. By early 2012, the box will be cleared by function, performance, thermal stress, mechanical and if required .a thermal vacuum test. This corresponds to IXO/EM box, in TRL-6.

3.4 HXI-D

The HXI-D is in principle reusing the same design as those of ASTRO-H/HXI, with a few modifications. Thus, it reaches TRL5 by the TRR-2 scheduled in mid-2011, and TRL-6 by early 2012, when the system is delivered to the ASTRO-H spacecraft.

Major technologies:

3. CPU boards with CPU and FPGAs, controlling the DIO boards in HXI-E, generating science mission packets, and communicate with spacecraft network for command control and telemetry transfer.
4. Power supply unit (PSU) for HXI-D.

Current Status:

For the ASTRO-H project, all the major technologies are in the status of TRL-4. All systems have been successfully operated in laboratory environment.

Future plan (by mid-2011):

EM (models for electrical test and performance verification) units of CPU boards and PSU will be fabricated and tested by early-2010. Function test as well as qualification tests (thermal, and if required, vacuum and mechanical) will be performed by mid-2010.

ASTRO-H/FM fabrication will start at late-2010, and basic function test will be done by mid-2011. By early 2012, the box will be cleared by function, performance, thermal stress, mechanical and if required .a thermal vacuum test. This corresponds to IXO/EM box, in TRL-6.