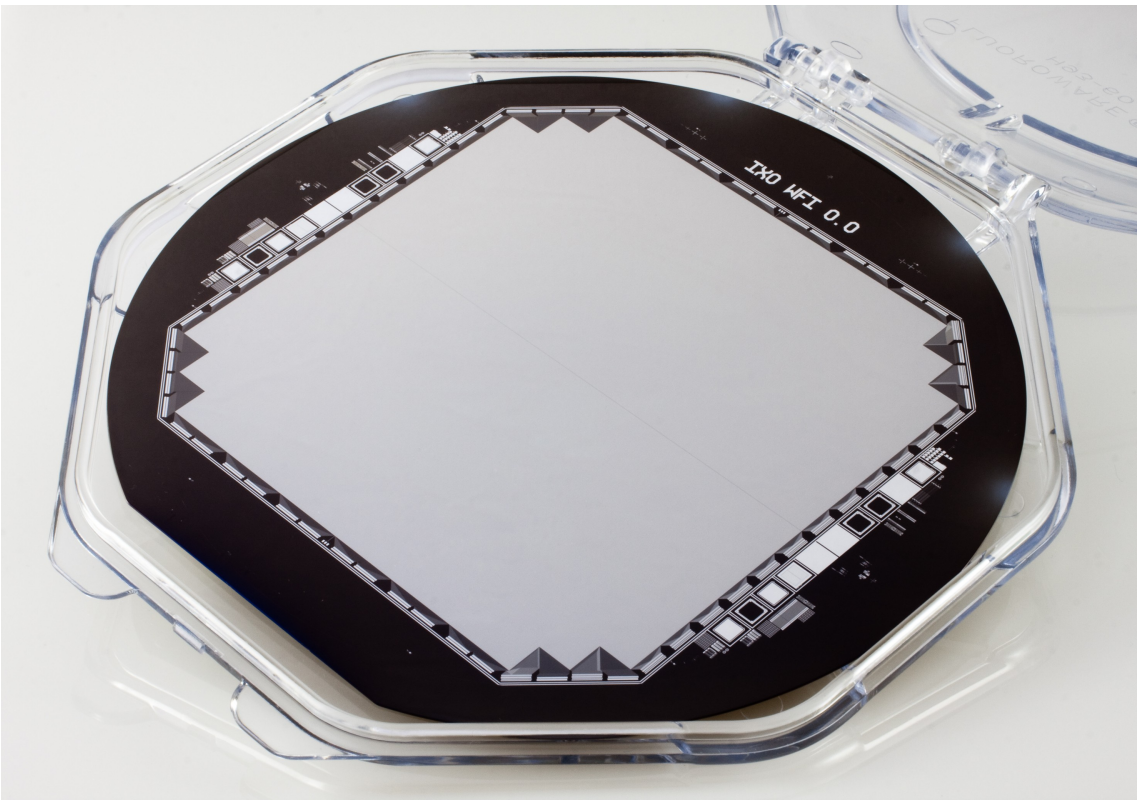
WFI Technology Development Roadmap



Prepared by

The WFI Instrument Consortium

1 Introduction

The Wide Field Imager (WFI) for IXO is an imaging X-ray spectrometer based on the concept of an active pixel sensor (APS). Although its invention is dating back to the late eighties the first operational systems were only tested in the beginning of the new millennium, just after the successful launch of XMM-Newton. Small matrices were first built in formats of 64 x 64 and pixel sizes of 75 x 75 μm^2 with sensitive areas of 4.8 x 4.8 mm^2. Since then a large variety of devices were designed, fabricated and tested with pixel sizes from 24 x 24 μm^2 up to 625 x 625 μm^2 and formats of 512 x 256 and sensitive areas up to 10 cm^2. Being used for the detection of particle tracks in high energy physics, photon detection in the optical and X-rays the devices were fabricated as junction field effect transistors (JFETs) as well as metal oxide silicon field effect transistors (MOSFETs). New concepts have been successfully tested such as gateable devices on a nanosecond scale as well as repetitive non-destructive readout schemes with noise figures below 0.2 electrons noise (rms). All of that means that a broad bandwidth of structures were invented, modelled and characterized in a quantitative way.

We will briefly describe the current development status of the devices, the systems and the WFI as a high resolution X-ray camera for IXO. The IXO WFI development is heavily supported by the realization of the X-ray cameras for eROSITA (384 x 384, 75 x 75 μm^2 pnCCDs, 7 flight cameras, 2012), the BepiColombo MIXS experiment (DEPFET macropixel detector, 64 x 64, 300 x 300 μm^2, 2 flight cameras, 2013). Also work on the SIMBOL-X low energy detector (DEPFET macropixel detector, 128 x 128, 625 x 625 μm^2) adds to the heritage, although SIMBOL-X has subsequently been discontinued. Therefore environmental testing and system design is quite advanced. In the instrument development plan we will outline the achievements as well as the open questions and critical issues.

As this document is strictly related to the payload definition document, we invite the reader to read the PDD wherever more technical details are required for a deeper understanding.

2 Instrument concept

The IXO wide field imager is an imaging X-ray spectrometer with a large field of view. The purpose of the WFI is to provide images in the energy band 0.1-15 keV[1], simultaneously with spectrally and time resolved photon counting. The device consists of an array of DEPFET (Depleted p-channel FET) active pixels integrated onto a common silicon bulk. Based on the principle of sideways depletion, these devices combine the advantages of sideways depleted silicon detectors with new benefits arising from the innovative DEPFET concept.

The DEPFET is a combined detector-amplifier structure. Every pixel consists of a p-channel MOSFET, which is integrated onto a fully depleted silicon bulk. By means of the sideways depletion principle, the bulk is fully depleted. With the help of an additional deep-n implantation, a potential minimum, the so-called internal gate, for electrons is generated and laterally constrained to the region below the transistor channel. Incident X-rays interact with the bulk material, and the resulting charge is separated; while holes drift to the most nearby p-contact, the electrons are collected in the internal gate of the adjacent pixels. There, their presence influences the conductivity of the MOSFET channel; sensing the increase of channel conductivity of the MOSFET is therefore a measure of the quantity of collected charge.

[1]The energy range 0.1-15 keV is consistent with the IXO Science Requirements Document. There are indications that the WFI could provide useful scientific data down to 0.05 keV, although such an extension of the energy range would impact on cost and complexity due to stricter contamination and cleanliness requirements.

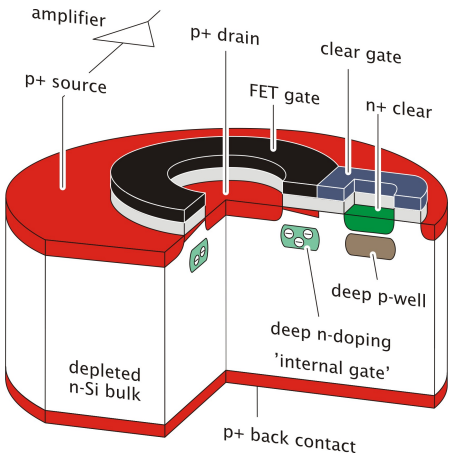


Fig. 1.: Cross cut through a circular DEPMOSFET pixel as implemented as prototype for IXO. The bulk thickness is 450 micron.

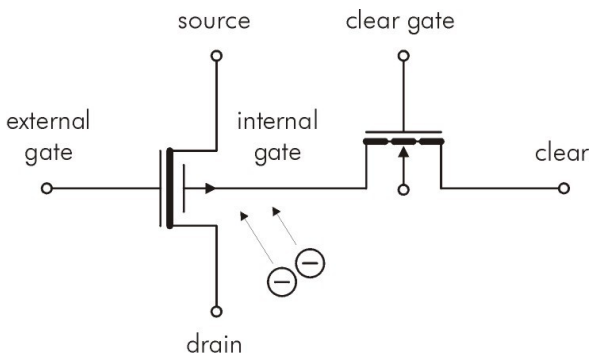


Fig. 2.: Schematic representation of a DEPMOSFET pixel as a combination of a dual-gate p-channel MOSFET and the parasitic n-channel ClearFET structure.

As the internal gate persists regardless of the presence of a transistor current, the pixel can be turned off during a specified exposure time, and only turned on for readout. The amount of integrated charge can then be sensed by turning on the transistor current, measuring the conductivity, removing the charge completely by a nearby parasitic n-channel MOSFET, the so-called ClearFET, and measuring the conductivity again. Considering the linear response of the channel conductivity to charge in the internal gate, calculating the difference is a measurement of the integrated charge.

The prototype devices designed for IXO have circular transistor geometry. A cutaway of a DEPMOSFET pixel and its schematic circuit representation are shown in Figure 1. and 2. Figure 3. shows a microscope photography of a fully processed matrix pixel.

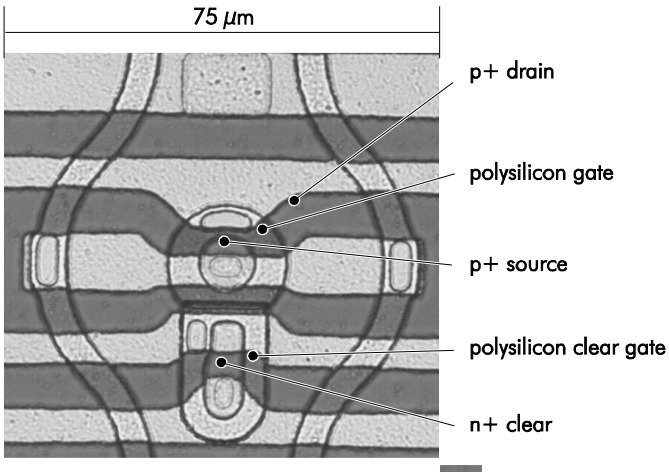


Fig. 3.: Microphotograph of a DEPFET pixel structure. In the bottom half, the ClearFET structure can be seen. At the periphery, column-separating structures are visible. The gate width of these structures is < 5 micron, the gate circumference is ~ 45 micron.

Various options exist for the integration of a matrix of DEPMOSFET pixels. Basically, every pixel could be individually addressed and read out at arbitrary times. For the sake of speed and simplicity and considering the accommodation of the HXI behind the WFI, a simple interconnection scheme was chosen, which provides for a row-wise readout in a “rolling shutter” like readout mode. In spite of its simplicity, this mode still allows for a large variety of useful readout modes.

Each X-ray photon is measured by detection in a single pixel, of photoelectrons liberated on X-ray absorption. The pixel size is smaller than the optics resolution element, giving good spatial resolution. The energy resolution is limited by silicon photoelectron statistics and timing resolution according to readout speed. The field of view is 18 arcmin (active detector area is 100 x 100 mm^2).

The benefits taken from using a DEPFET based sensor are listed below.

- The DEPFET is a fully depleted device, the full wafer thickness of 450 µm helps to increase the quantum efficiency in the range around 15 keV.
- DEPFET based devices are sideways depleted devices, which provides for an unobstructed, homogeneous entrance window with 100% fill factor and excellent QE in the low energy range.
- The local charge storage capability allows for a large variety of flexible readout modes, which allow observing objects in a large range of brightness without being limited by pileup.
- The very low readout capacitance of the DEPFET allows for very low readout noise and thus excellent energy resolution even at high speed.
- The sensor is area efficient compared to CCD based sensors, as no frame store area is needed.
- The sensor has an extremely low deadtime compared to CCD based sensors, as no charge transfer is needed.
- The sensor is radiation hard and power efficient, as the pixels are turned on only during readout.

2.1 Instrument performance specifications

According to the Science Requirements Document (SRD), the following scientific objectives are to be met by the WFI:

- Detection, location and broad band colours of faint AGN counterparts
- Spatially resolved spectra of extended objects
- Spectral investigation of moderately bright point sources to time resolution ~millisecond

The resulting performance requirements derived from these objectives have been listed in table 1. The given numbers are the current baseline, and wherever changes are possible, the decision drivers are indicated. The main open issues are the pixel size and array geometry, which are driven by the PSF size of the mirrors. If the PSF is smaller than about 4”, a pixel size smaller than 100 µm can be considered. The current device area (10 x 10 cm^2) meets the IXO requirements for the field of view (18 x 18 arcmin) and is the largest that can be accommodated by a monolithic device on a 6-inch wafer.

A more complete description of the DEPFET camera can be found in the payload definition document.

2.2 Performance figures and specification

The scientific performance figures relevant to the IXO mission are already close to the initial scientific specifications. But of course that does not mean that the instrument development is coming to an end. To match the science requirements and to build a space qualified instrument still needs intensive research and development – in the hardware domain as well as in software. The preparation of the space missions eROSITA, BepiColombo with the launch of the first of those missions in 2012 forces us to do mechanical, thermal, electrical and performance tests at an early stage. But as the detectors are differing and the mission concepts are quite dissimilar the entire system engineering needs to be repeated.

Requirement	Specification	Comments	Achieved
Device dimensions			
Area	10 x 10 cm^2	Integrated on monolithic 6" wafer	3.2 x 3.2 cm^2
Thickness	450 µm	For good QE at high energies	450 µm
Pixel size	100 x 100 μm^2	Up to 100 x 100 μm^2 possible for monolithic device. Depends on optics PSF.	from 24 x 24 μm^2 to 500 x 500 μm^2
Array dimension	1024 x 1024	For pixel sizes larger than 100 µm either monolithic concept or array dimension has to be abandoned. Baffle and FoV problem?	max. 1024 x 256 tested: 256 x 256 typical: 64 x 64
Spectroscopy			
Energy resolution			
@ Mn-Kα 5.9 keV	125 eV FWHM		125 eV
@ C-Kα 282 eV	50 eV FWHM		45 eV
Readout noise	3-5 e^- ENC		3 e^- (rms)
Readout timing			
Readout time / frame	1 – 1.5 ms	Depends on front-end electronics performance	
Processing time / row	2 – 3 µs		4 µs
Raw data rate	1.6 GByte / s	Final data rate depends on pre-processing	
Quantum efficiency			
Fill factor	100 %	No dead areas	100 %
QE @ C-Kα (282 eV)	33 %	Depending on implementation of	90 %
QE @ Si-Kα (1.74 keV)	93 %	Optical blocking filter	100 %
QE @ Cu-Kα (8.04 keV)	100 %		100 %
QE @ 10 keV	96 %		98 %
QE @ 20 keV	45 %		30 %

Table 1: Expectations and achievements

3 Technology Roadmap

In the following, we will very briefly describe the roadmap to achieving a Technical Readiness Level of 6 over the major components – detector, front-end electronics and data acquisition – of the WFI.

	Name	Duration	Start	Predecessors	Resource Names
1	TRL 5	0 days	2/11/11 5:0...	27;9;13	
2	TRL 6	0 days	1/13/12 5:0...	52;39;38;31;14	
4	Instrument Definition Rev	0 days	11/13/09 9:...		
5	Instrument TRL Rev.	0 days	5/3/10 8:00 ...		
6	Instrument Preliminary Req. Rev.	0 days?	5/3/10 8:00 ...		
7	ASICS	210 days?	7/16/09 8:0...		
8	VBLA / ASTEROID long-term us...	84 days?	7/16/09 8:0...		
9	ASIC rad-hardness tests	126 days	11/11/09 8:...	8	
10	DAQ	496 days?	7/16/09 8:0...		
11	Iga-Board DAQ development	55 days?	7/16/09 8:0...		
12	SUMO-DAQ development	126 days	10/1/09 8:0...	11	
13	XL new-age operation	63 days	3/26/10 8:0...	12	
14	FPGA-based serial preproc (S...	252 days	6/23/10 8:0...	13	
15	Detector Development	642 days?	7/30/09 8:0...		
16	XL Device	189 days?	8/1/09 8:00...		
17	XL DAQ Adaption	63 days?	8/1/09 8:00 ...		
18	XL AIV	21 days?	8/1/09 8:00 ...		
19	Early XL operation	63 days?	10/29/09 8:...	17;18	
20	XL Characterisation	63 days?	1/26/10 8:0...	19	
21	XXL Device	379 days?	9/1/09 8:00...		
22	XXL hybrid development	63 days?	9/1/09 8:00 ...	22	
23	XXL hybrid production	84 days	11/27/09 8:...	23	
24	XXL AIV	21 days?	3/25/10 8:0...	23	
25	Early XXL operation	63 days?	6/23/10 8:0...	19;24;13	
26	XXL Characterisation	63 days?	9/20/10 8:0...	25	
27	XL / XXL Irradiation study	42 days?	12/16/10 8:...	26	
28	IQ Device	642 days?	7/30/09 8:0...		
29	PXD7 Layout	12 days?	7/30/09 8:0...	30SF	
30	IQ Production	336 days?	8/17/09 8:0...		
31	IQ Yield determination	63 days?	11/30/10 8:...	30	
32	IQ hybrid concept dev	21 days?	11/27/09 8:...	22	
33	IQ hybrid development	63 days?	12/28/09 8:...	32	
34	IQ hybrid manufacturer rese...	42 days?	12/28/09 8:...	32	
35	IQ hybrid production	84 days?	3/25/10 8:0...	34;33;23	
36	IQ AIV	42 days?	2/25/11 8:0...	35;31	
37	Early IQ operation	63 days?	4/26/11 8:0...	36	
38	IQ Characterisation	63 days?	7/22/11 8:0...	37	
39	IQ irradiation study	63 days?	10/19/11 8:...	38	
40	Vibration & TV	294 days?	3/25/10 8:0...		
41	IF hybrid pre-study	42 days?	3/25/10 8:0...	33;29	
42	IF hybrid manufacturer rese...	42 days?	7/21/10 8:0...	41;35	
43	IF hybrid dummy production	42 days?	9/17/10 8:0...	42	
44	IF FPA protoype dev	42 days?	5/24/10 8:0...	41	
45	FPA thermal modelling	63 days?	5/24/10 8:0...	44SS	
46	FPA thermal modelling	63 days?	5/24/10 8:0...	44SS	
47	FPA mech prototype produc...	84 days?	8/19/10 8:0...	44;45;46	
48	IF dummy design	21 days	5/24/10 8:0...	41	
49	IF dummy production	21 days	6/22/10 8:0...	48	
50	IF prototype assembly	63 days?	12/15/10 8:...	43;49;47	
51	TV tests	21 days	3/14/11 8:0...	50	
52	Vibration tests	21 days	4/12/11 8:0...	51	

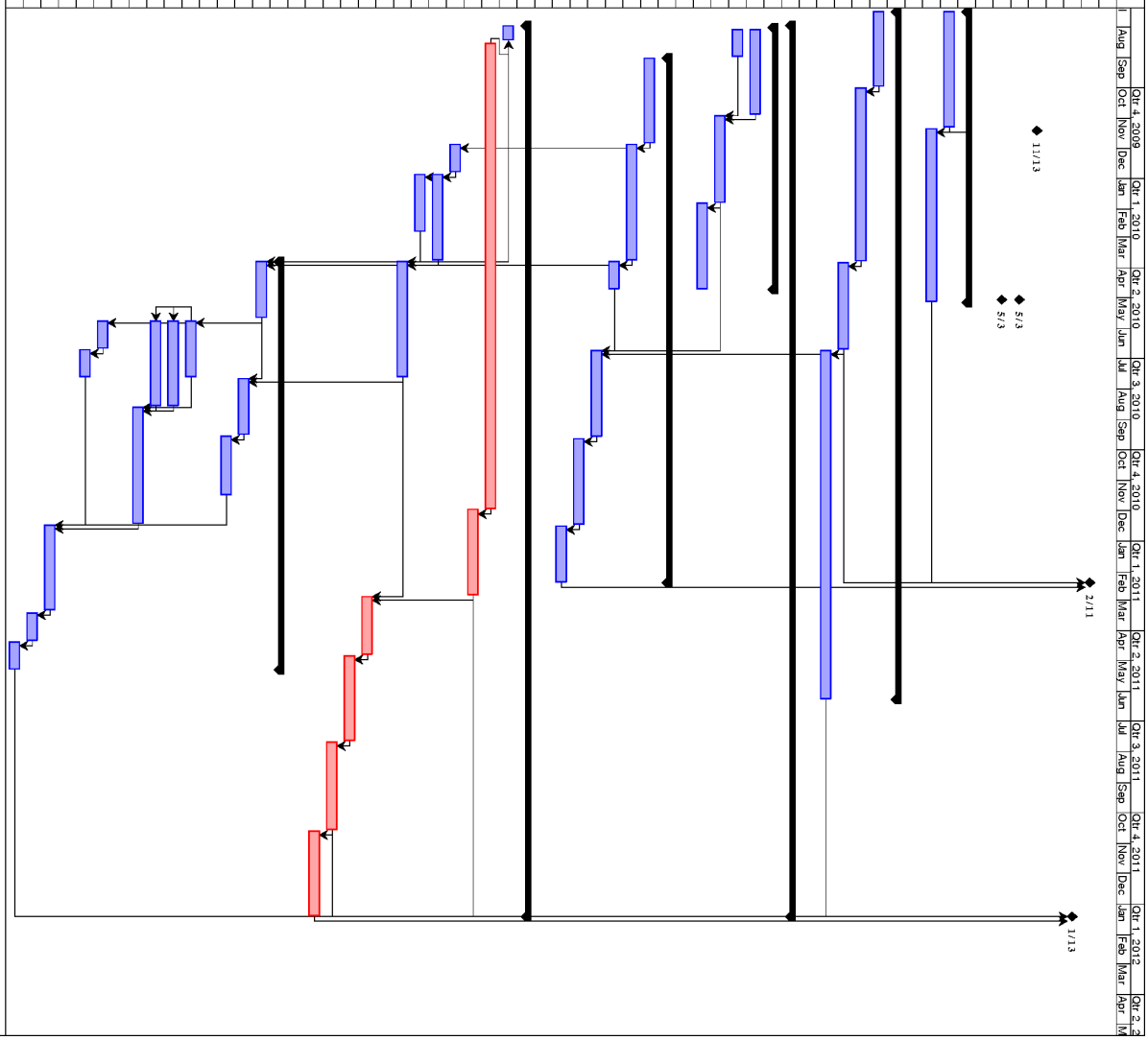


Fig. 4: Technology Roadmap Schedule

3.1 Detector

Detector development is the largest work package in the roadmap to TRL 6. Critical scaling issues to achieve TRL 6 are pixel count and detector area.

As the WFI will be read out in multiple 128 x 512 pixel sectors, prototypes demonstrating WFI sector (128 x 512 pixel "XXL" device) and multiple-node readout (256 x 256 pixel "XL" devices and "XXL" devices) will address readout scaling. "XL" and "XXL" devices have already been produced. Each sensor geometry needs a hybrid ceramic circuit board. A hybrid for operation of "XL" devices has already been developed and manufactured. For "XXL" devices, a corresponding hybrid needs to be developed. For both types of devices, the test-bench needs to be adapted for multi-node readout.

Production and operation of prototype devices of full logical and physical WFI quadrant dimensions (512 x 512 pixels, 100 x 100 μm^2 pixel size, "IQ" device) will allow addressing of large area yield scaling. The production of "IQ" devices is the longest individual task of this roadmap and defines the overall critical path. As the WFI quadrant-size "IQ" devices cannot be accommodated by current hybrid designs due to their size, hybrid development will take longer for "IQ" devices than for "XXL" devices. However, as this can be performed in parallel to "IQ" device production it is not on the critical path.

All sensor prototypes are routinely operated in baseline WFI thermal conditions and under vacuum conditions. Irradiation studies on various detector formats ("XL" & "IQ") plus vibration and T/V testing on full-scale FPA models complete demonstration of operations under critical environment conditions. For vibration testing, a full-scale hybrid model needs to be developed. Experience from the quadrant-size hybrid development for "IQ" devices will be used in the design.

3.2 ASIC development

Charge accumulates during illumination of the DEPFET in the internal gate, enhancing the conductivity of the MOSFET channel. To determine the amount of charge stored in the internal gate, the current through the pixel is sensed, the accumulated charge is cleared out of the internal gate, and the current is sensed again. The difference between these two measurements corresponds to the accumulated charge.

The current standard hardware implementation of this readout scheme is the CAMEX ASIC. The CAMEX is a 64-channel readout chip including 64 parallel ac-coupled voltage pre-amplifiers and 64 filter amplifiers based on 8-fold correlated double sampling. In the CAMEX readout scheme, the sensor-internal DEPFET is operated as source-follower.

As the speed necessary for WFI operation is near the maximum achievable with CAMEX, two new ASICs, VELA and ASTEROID have been developed. VELA uses a direct integration/de-integration of the current through the DEPFET and a filter with a trapezoidal weighting function. ASTEROID uses the same trapezoidal filter, but operates as a source-follower. As CAMEX and VELA/ASTEROID have been designed in a pin-compatible layout, a change of the readout ASIC can be performed at any time. As VELA and ASTEROID continue to replace CAMEX as default read-out ASICs in all DEPFET operations, they are being operated continuously in critical test environments and can be considered TRL 4. Further radiation hardness studies (total ionizing dose, latch-up, single-event upset) and inclusion in FPA-level T/V tests and vibration tests will demonstrate operation under critical environment conditions and justify TRL 6.

3.3 DAQ chain

As the raw data-rate of the WFI is going to be extremely high (~1.5 Gbyte/s), data-reduction at an early stage in the DAQ chain is critical. The data-reduction will be performed in two stages: stream-based data reduction that just needs information about the data of individual pixels, and image-based data reduction that needs recombined frames. Both steps are going to be performed by a three cascaded FPGA based data processors: Eight ADC Cluster FPGAs perform stream data reduction, two Hemisphere Preprocessors and one Frame Builder perform image based data reduction.

Currently, the data reduction pipeline exists in software and is routinely used in the lab when operating DEPFET prototype devices. Currently a new DAQ chain is under development. This will allow simultaneous multi-node readout. Additionally it will serve as a breadboard for FPGA-based data-reduction. Multi-node read-out and FPGA-based serial preprocessor prototype will address HW scalability and demonstrate a prototype implementation of SW on a full-scale realistic problem.